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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,928	12/12/2003	Alexander Kalnitsky	55123P231D	2239

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EXAMINER	
BREWSTER, WILLIAM M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/734,928	KALNITSKY ET AL.	
	Examin r	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears n the cover sheet with the c rresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *041904*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 23-30, 32-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Dunn et al., U.S. Publication No. 2002/0132438 A1.

Dunn anticipates a bipolar transistor, comprising:

in fig. 26, a substrate 52 having a collector region, the collector 57 region being a collector terminal, under 104, p. 4, ¶ 66;

a first epitaxial silicon layer 58 on a surface of the substrate, p. 4, ¶ 66;

an emitter stack 130 on the first epitaxial silicon layer, the emitter stack being an emitter terminal, p. 4, ¶ 73;

a second epitaxial silicon layer 120 on portions of the first epitaxial silicon layer located outside the emitter stack;

limitations from claim 25: wherein the emitter region further comprises a nitride spacer 124 directly adjacent to the polysilicon emitter, p. 4, ¶ 67;

limitations from claim 31: in fig. 26, wherein the emitter stack includes a first oxide layer 112 on the first epitaxial silicon layer, p. 4, ¶ 67; a first nitride layer 124 on the first oxide layer, p. 4, ¶ 71; a second oxide layer 122 on the first nitride layer, p. 4, ¶ 70; ions incorporated in the polysilicon to form the polysilicon emitter, p. 4, ¶ 66;

limitations from claim 35: in fig. 26, wherein the polysilicon emitter structure has a first portion providing an emitter base junction, between structures labeled 112, a second portion providing conduction, between structures labeled 124, and a third portion providing an emitter contact region, between structures labeled 132;

limitations from claims 24, 36: wherein the first portion of the polysilicon emitter structure has a width A, between structures labeled 112, the second portion of the polysilicon emitter structure has a width B, between structures labeled 124,

differing from A, the third portion of the polysilicon emitter structure has a width C, between structures labeled 132 differing from A and C;

limitations from claim 37: wherein the width C is greater than the width B which is greater than the width A;

better illustrated in fig. 13, wherein a region of the first epitaxial silicon layer located under the emitter stack is an intrinsic base region 58i, p. 3, ¶ 54, and a region of the second epitaxial silicon layer on portions of the first epitaxial silicon layer located outside the emitter stack being a raised extrinsic base region, p. 4, ¶ 68-69, p. 3, ¶ 60; wherein the raised extrinsic base region has a thickness greater than a thickness of the intrinsic base region: intrinsic base region between about 500 Å and about 3000 Å, p. 3, ¶ 54, extrinsic base region, at least about 1000 Å, p. 4, ¶ 68;

limitations from claims 23, 33, 34: wherein the extrinsic base region has a thickness X and the intrinsic base region has a thickness y, and wherein X is greater than Y, see above, and the extrinsic base region is raised relative to the intrinsic base region;

and wherein the intrinsic base region and the raised extrinsic base region provide a base terminal of the bipolar transistor with lower resistivity, p. 1, ¶ 15;

limitations from claims 27, 30: wherein the first epitaxial layer is a p-type Si, SiGe or SiGe:C epitaxial layer, SiGe, p. 4, ¶ 66, and the second epitaxial layer is a selectively deposited heavily p-type doped Si epitaxial layer or a selectively deposited heavily p-type doped SiGe epitaxial layer, p. 4, ¶ 68;

limitations from claims 28, 32: wherein the bipolar transistor is a SiGe or SiGe:C: SiGe, p. 4, ¶ 66 npn bipolar transistor: N emitter, p. 4, ¶ 72; P base, pp. 2-3, ¶ 50; N collector, pp. 2-3, ¶ 50.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dunn as applied to claims 23-30, 32-37 above.

The method limitations of claim 31, "ions implanted through an emitter window in the second oxide layer and the first nitride layer to form a polysilicon emitter" are not given patentable weight in a device claim as they are "product by process".

Initially, with respect to claims a **"product by process"** claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15. See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554, does not deal with this issue); In re Fitzgerald 205 USPQ 594, 596 (CCPA); In re Marosi et al , 218 USPQ 289 (CAFC); and In re Thorpe et al, 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the patentability of the final product per se which must be determined in a **"product by process"** claim, and not the patentability of the process,

and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Brewster

8 July 2004
WB